In the Claims:

1. (Currently Amended) A method of fabricating a CMOSFET comprising:

forming a plurality of gate patterns on a first region and a second region of a semiconductor substrate; then

forming gate spacers on both sidewalls of the gate patterns; then

forming a first impurity region of a first conductivity type in the first region of the semiconductor substrate; then

removing the gate spacers exposed at the first region; then

forming a second impurity region of the first conductivity type in the first region from which the gate spacers have been removed, the second impurity region having shallower depth than the first impurity region;

forming a third impurity region of a second conductivity type in the second region; then

removing the gate spacers exposed at the second region; and then

forming a fourth impurity region of the second conductivity type in the second region, the fourth impurity region having shallower depth than the third impurity region;

wherein the first impurity region has higher impurity concentration than the second impurity region; and

wherein the fourth impurity region has impurity concentration as high as the third impurity region.

2.-3. (Canceled)

4. (Original) The method of fabricating the CMOSFET of claim 1,

wherein the first impurity region is formed in the first region, using the gate pattern and the gate spacers as an ion implantation mask;

wherein the second impurity region is formed in the first region, using the gate pattern as an ion implantation mask;

wherein the third impurity region is formed in the second region, using the gate pattern and the gate spacers as an ion implantation mask; and

wherein the fourth region is formed in the second region, using the gate pattern as an ion implantation mask.

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5. (Currently Amended) The method of fabricating the CMOSFET of [[the]] claim 1,

wherein the gate spacers comprise at least one selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, silicon carbide and silicon.

6. (Original) The method of fabricating the CMOSFET of claim 1,

wherein removing the gate spacers at the first region and second region are performed by isotropic etching.

7. (Currently Amended) The method of fabricating the CMOSFET of claim 1, wherein, before forming the third impurity region, a first HALO ion implantation is performed to form a first HALO region,

wherein the first HALO region is formed to cover sides of the first impurity region beneath the second impurity region.

8. (Original) The method of fabricating the CMOSFET of claim 1, wherein after forming the fourth impurity region, a second HALO ion implantation is performed to form a second HALO region; and

wherein the second HALO region is formed to cover sides of the third impurity region beneath the fourth impurity region.

9.-30. (Canceled)

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